

(19)



JAPANESE PATENT OFFICE

PATENT ABSTRACTS OF JAPAN

(11) Publication number: **01106456 A**

(43) Date of publication of application: **24.04.89**

(51) Int. Cl

**H01L 23/50**  
**H01L 23/28**

(21) Application number: **62263435**

(22) Date of filing: **19.10.87**

(71) Applicant: **MATSUSHITA ELECTRIC IND CO LTD**

(72) Inventor: **KURODA HIROSHI  
TAKASE YOSHIHISA**

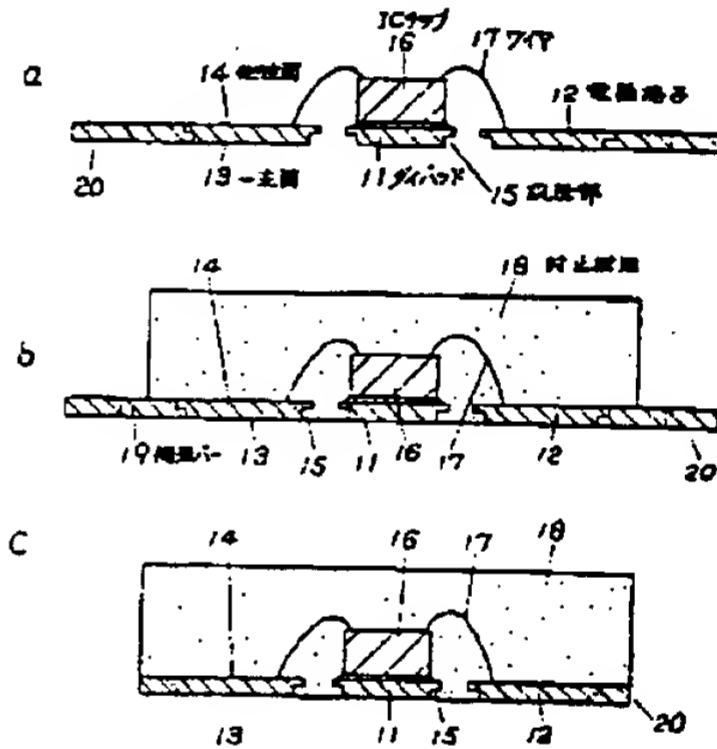
(54) SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

COPYRIGHT: (C)1989,JPO&Japio

(57) Abstract:

PURPOSE: To make an electrode terminal not to come off due to external force and thermal strain by providing the end surface of a lead frame substrate with a stair part having more than one step and performing molding with sealing resin in a shape of covering the stair part.

CONSTITUTION: An IC chip 16 is mounted on the other main surface 14 of a die pad 11, and a pad of the IC chip and the other main surface 14 of an electrode terminal 12 are bonded with a wire 17 so as to be continuously molded with sealing resin 18 on the almost level with one main surface 13 by a transfer method so that the electrode terminal and the main surface 13 of the die pad 11 may be exposed. At this time, a stair part 15 provided on a lead frame 20 is also covered with sealing resin 18. Thereby, a reinforcing bar 19 exposed to an end surface of sealing resin 18 is also of the same projection type so as to have very strong structure against coming-off even to external force.



Japanese Kokai Patent Application No. Hei 1[1989]-106456

---

Job No.: 2098-96421

Ref.: 022111-000100US

Translated from Japanese by the Ralph McElroy Translation Company  
910 West Avenue, Austin, Texas 78701 USA

JAPANESE PATENT OFFICE  
PATENT JOURNAL (A)  
KOKAI PATENT APPLICATION NO. HEI 1[1989]-106456

Int. Cl.<sup>4</sup>: H 01 L 23/50  
23/28

Sequence Nos. for Office Use: G-7735-5F  
A-6835-5F

Filing No.: Sho 62[1987]-263435

Filing Date: October 19, 1987

Publication Date: April 24, 1989

No. of Inventions: 1 (Total of 4 pages)

Examination Request: Not filed

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

Inventors: Hajime Kurada  
Matsushita Electric Industrial Co.,  
Ltd.  
1006 Oazakadoma, Kadoma-shi,  
Osaka-fu

Yoshihisa Takase  
Matsushita Electric Industrial Co.,  
Ltd.  
1006 Oazakadoma, Kadoma-shi,  
Osaka-fu

Applicant: Matsushita Electric Industrial Co.,  
Ltd.  
1006 Oazakadoma, Kadoma-shi,  
Osaka-fu

Agents: Toshio Nakao, patent attorney, and 1  
other

[There are no amendments to this patent.]

## Claim

A semiconductor integrated circuit device characterized by the following facts: the area of one principal surface of a lead frame having plural electrode terminals is smaller than that of the other principal surface; the cross-sectional shape of the lead frame has at least one step; a semiconductor integrated circuit is mounted on the other principal surface; and, with at least said one principal surface having the electrode terminals exposed, molding is performed with a sealing resin so that the resin is nearly flush with said one principal surface.

## Detailed explanation of the invention

### Industrial application field

The present invention pertains to a semiconductor integrated circuit device containing a packaged semiconductor integrated circuit.

### Prior art

An IC card that can be used as a portable information file has a semiconductor integrated circuit device with memory and microprocessor units embedded in a portion of the card. By means of the operation of a reader/writer, information can be written and read or erased. According to the ISO code, the maximum thickness of the card is 0.84 mm. Naturally, the semiconductor integrated circuit device must be even thinner and the thickness must be highly precise.

The conventional substrate for the semiconductor integrated circuit device is usually a double-sided substrate using glass epoxy resin as the base material. However, glass epoxy substrates cannot sufficiently satisfy the demands on thickness precision required for semiconductor integrated circuit devices for IC cards.

Consequently, a semiconductor integrated circuit device for IC cards has been proposed using a lead frame instead of a glass epoxy substrate as a substrate with better thickness precision so as to improve the thickness precision for the overall thickness of the semiconductor integrated circuit device. The structure of this semiconductor integrated circuit device for IC cards can be explained with reference to Figure 4.

For lead frame (8) having plural electrode terminals (1) and die pad (2), IC chip (3) is mounted on said die pad (2), the pad (not shown in the figure) of said IC chip (3) and said electrode terminals (1) are connected by wires (4). With at least one principal surface (5) of said electrode terminals (1) exposed, molding is performed with sealing resin (6) so that the resin is nearly flush with said one principal surface (5) using a transfer molding method.

However, said one principal surface (5) of said electrode terminals (1) is exposed to the outer side, and only one side containing the thin side surface of said electrode terminals (1) contacts said sealing resin (6). Usually, in order to improve the mold releasing property from molding dies in transfer molding methods, a mold releasing agent is added to said sealing resin (6). Naturally, adhesion between said electrode terminals (1) and said sealing resin (6) is not good. Methods for solving this problem include roughening the other principal surface (7) that contacts said sealing resin (6), and making the area of one principal surface (5) of said electrode terminals (1) smaller than the area of the other principal surface (7) (the edge has a tapered, truncated-trapezoid-shape), which improves adhesion.

#### Problems to be solved by the invention

Due to the limitation on the total thickness of the semiconductor integrated circuit device, the thickness of lead frame (8) used in the semiconductor integrated circuit device is usually 0.15 mm or less. However, in order to improve the adhesion between sealing resin (6) and the other principal surface (7) of lead frame (8), the cross section of lead frame (8) is processed into a tapered shape, and lead frame (8) is covered with a small amount of sealing resin (6). However, the thickness of lead frame (8) is as small as 0.15 mm, so even if the end surface of lead frame (8) is partially covered with sealing resin (6), only about 0.15 mm in thickness is deposited. Even when the end surface is tapered, the adhesive strength of lead frame (8) with respect to sealing resin (6) cannot be increased significantly. Also, as pointed out above, a mold releasing agent is contained in sealing resin (6). Consequently, the adhesion with lead frame (8) is poor. For example, due to thermal strain occurring during the burn-in phase, lead frame (8) may be separated. In addition, after the transfer molding, the reinforcing bar of lead frame (8) is cut by dies nearly flush with the end surface of sealing resin (6) to form individual semiconductor integrated circuit devices. However, when the reinforcing bar is cut by dies to form a cut surface, certain burrs are formed, and it is impossible to form a cut surface that is flush with the end surface of sealing resin (6), and the cut surface protrudes slightly. When a card is formed in this way, when it is carried or in use, certain foreign objects may become caught on the burrs formed on the cut surface or on the electrode terminals themselves. As a result, the electrode terminals may become separated or deformed, leading to total loss of function of the IC card.

The purpose of the present invention is to solve the aforementioned problems of the conventional methods by providing a structure of the lead frame which can avoid separation, and thus failure, of the electrode terminals due to external forces, thermal strain, etc.

### Means to solve the problems

In order to solve the aforementioned problem, in the technical means of the present invention, the area of one principal surface of a lead frame is made smaller than the other principal surface; the cross section has a convex shape, and molding is performed with a sealing resin so that the resin is nearly flush with said one principal surface; and, for the end surface of the lead frame, almost the entire edge is covered with the sealing resin over a prescribed distance and thickness.

### Operation

In this constitution, since almost the entire edge of the electrode terminals is covered with a sealing resin, no external forces that could separate the electrode terminals can be applied, and no separation takes place in the electrode terminals due to thermal strain during the burn-in phase, etc. Consequently, highly reliable semiconductor integrated circuit devices can be obtained.

### Application example

In the following, an application example of the present invention will be explained with reference to the figures. Figures 2a and b illustrate the structure of the lead frame used in the present invention. Figure 2a is a top view, and Figure 2b is a cross-sectional view taken across A-A'. The lead frame is composed of die pad (11) and plural electrode terminals (12). The area of one principal surface (13) exposed on the opposite side of said die pad (11) and said electrode terminals (12) is smaller than the other principal surface (14), and convex-shaped step (15) is formed as the cross section of lead frame (20) at least in the region to be covered with a sealing resin. When the thickness of lead frame (20) is 0.15 mm, W of said step (15) is 0.5 mm, and D is 0.1 mm. The cross-sectional shape of said step (15) may include plural steps instead of one step. For the aforementioned structure of the lead frame, die pad (11) is connected to at least one of plural electrode terminals (12). As an example for preparing this lead frame (20), first of all, straight punching is performed on a press unit. Then, another set of dies is set on the same press unit and presses just the end surface of lead frame (20) to form step (15) with the prescribed dimensions. In another method, etching is used to form this same step (15). The explanation above is for a lead frame (20) having a die pad (11) that can carry an IC chip. However, it is also possible to use a lead frame having only electrode terminals (12) but without a die pad (11).

Figures 3a-c illustrate the manufacturing process of a semiconductor integrated circuit device using said step-profile lead frame (20). They are taken across A-A' of Figure 2. IC chip (16) is mounted on the other principal surface (14) of die pad (11), and the pad (not shown in the figure) of said IC chip (16) and the other principal surface (14) of said electrode terminals (12)

are connected by wires (17) (Figure 3a). Then, by means of a transfer molding method, where one principal surface (13) of said electrode terminals (12) and die pad (11) is exposed, molding is performed with sealing resin (18) so that the resin is nearly flush with said one principal surface (13) (Figure 3b). At this time, step (15) set on lead frame (20) is also covered with said sealing resin (18). In addition, dies are used to cut reinforcing bar (19) along the end surface of said sealing resin (18) to form individual semiconductor integrated circuit devices (Figure 3c). Figure 1 is an enlarged view of the electrode terminal portion of the aforementioned semiconductor integrated circuit device. According to Figure 1, one principal surface of electrode terminals (12) and sealing resin (18) are formed nearly flush with each other, and a portion of electrode terminals (12) embedded in sealing resin (18) is wider than the exposed one principal surface in this structure. In this way, step (15) formed on the end surface of electrode terminal (12) is completely covered by sealing resin (18), and reinforcing bar (19) exposed on the end surface of sealing resin (18) also has a convex shape, so that it is very resistant to separation due to external forces.

As explained above, wires (11) are used for connecting the pad of IC chip (16) to electrode terminals (12). However, the present invention is not limited to the wire bonding method. The flip-chip-bonding method using bumps may also be adopted. Also, at the same time, the other principal surface of lead frame (20) may be processed by etching, sandblasting, or the like to form a rough surface. In addition, when a lead frame (20) without a die pad (11) is used with IC chip (16) and set against electrode terminals (12), the die bonding resin for mounting IC chip (16) is naturally insulating.

#### Effects of the invention

For the semiconductor integrated circuit device in the present invention, one or several steps are formed on the end surface of the lead frame substrate, and a sealing resin is used for molding to cover the step. Consequently, the electrode terminals cannot be separated even by external forces, and the electrode terminals cannot be separated even by thermal strain during a burn-in phase or the like. That is, high reliability can be realized.

#### Brief description of the figures

Figure 1 is an enlarged oblique view of the electrode terminal portion in an application example of the semiconductor integrated circuit device of the present invention. Figures 2a and b are a top view and a cross-sectional view illustrating the structure of the lead frame used in the present invention, respectively. Figures 3a-c are cross-sectional views illustrating the manufacturing process of the semiconductor integrated circuit device in the present invention.

Figure 4 is a cross-sectional view illustrating the structure of the semiconductor integrated circuit device using a conventional lead frame.

- 12 Electrode terminal
- 13 One principal surface
- 14 Other principal surface
- 15 Step
- 16 IC chip
- 17 Wire
- 18 Sealing resin
- 19 Reinforcing bar
- 20 Lead frame

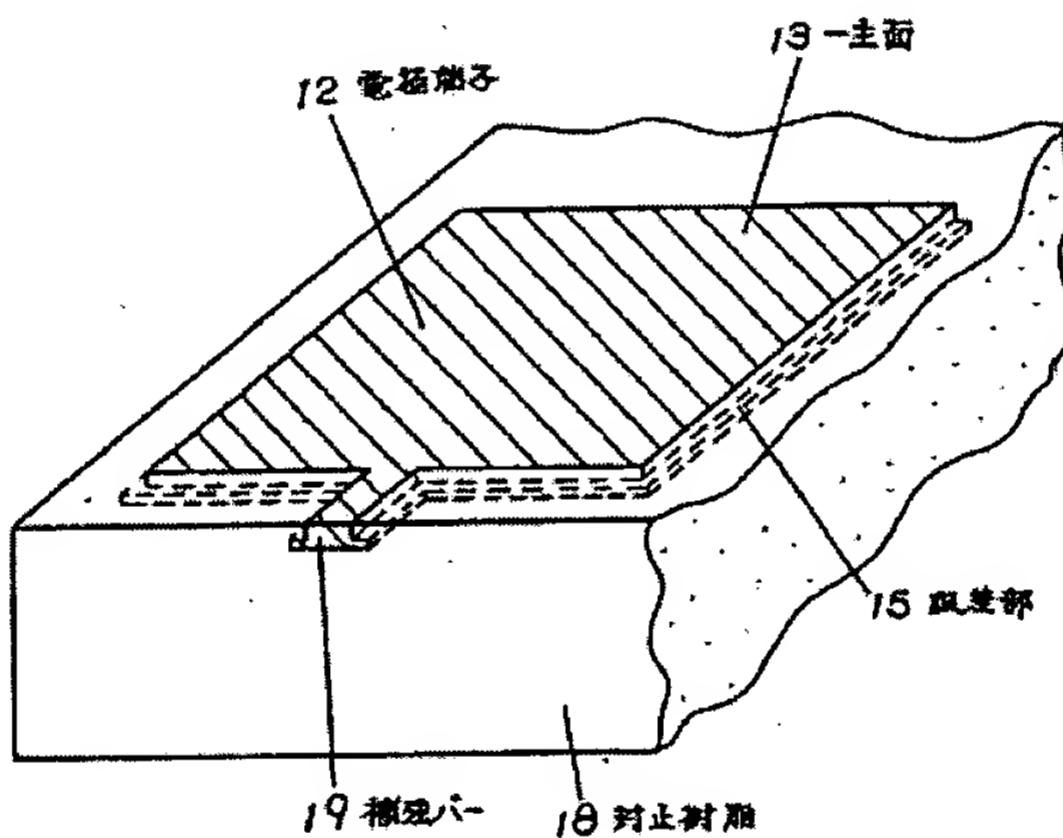


Figure 1

Key:

- 12 Electrode terminal
- 13 One principal surface
- 15 Step
- 18 Sealing resin
- 19 Reinforcing bar

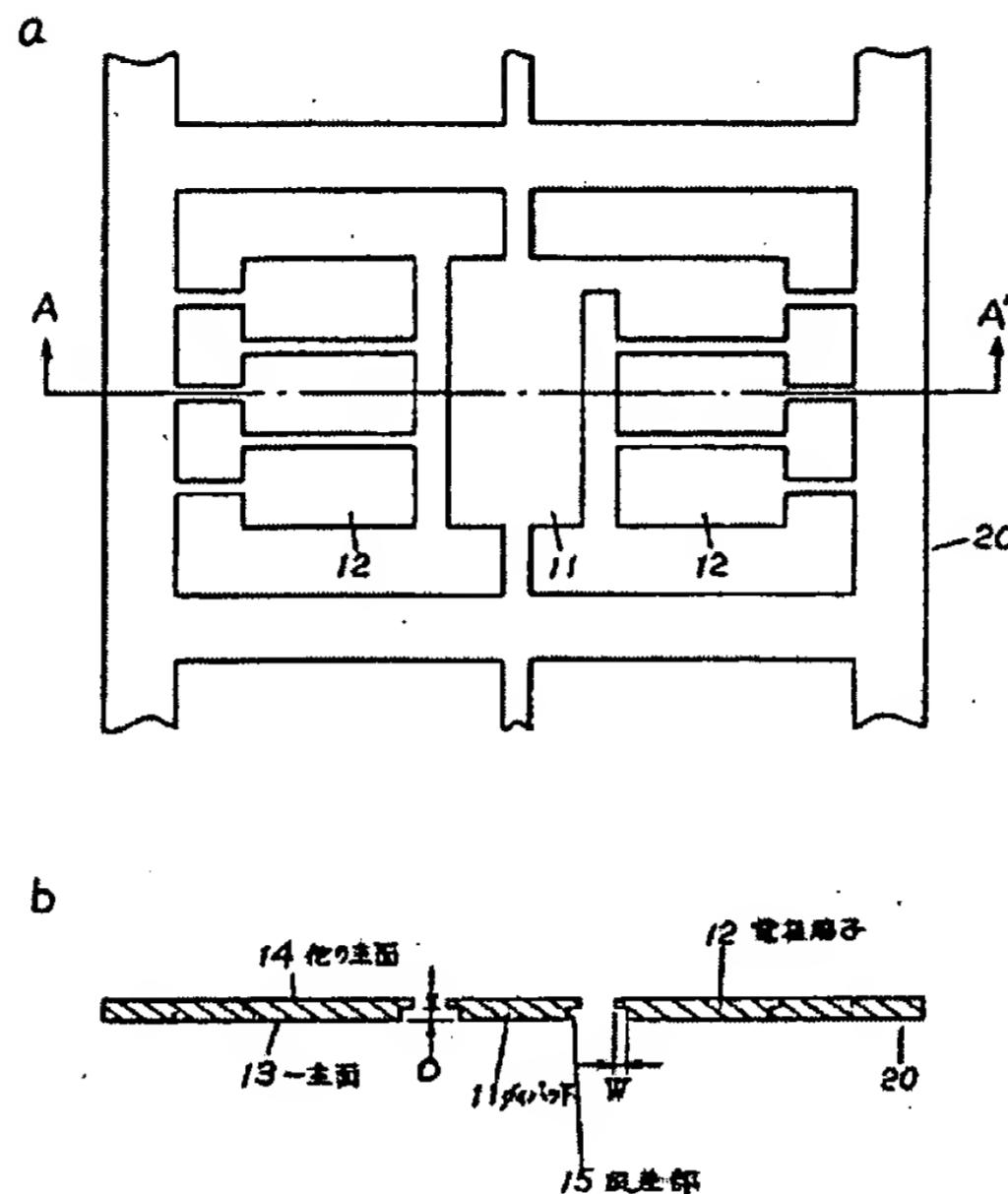


Figure 2

Key:

- 11 Die pad
- 12 Electrode terminal
- 13 One principal surface
- 14 Other principal surface
- 15 Step

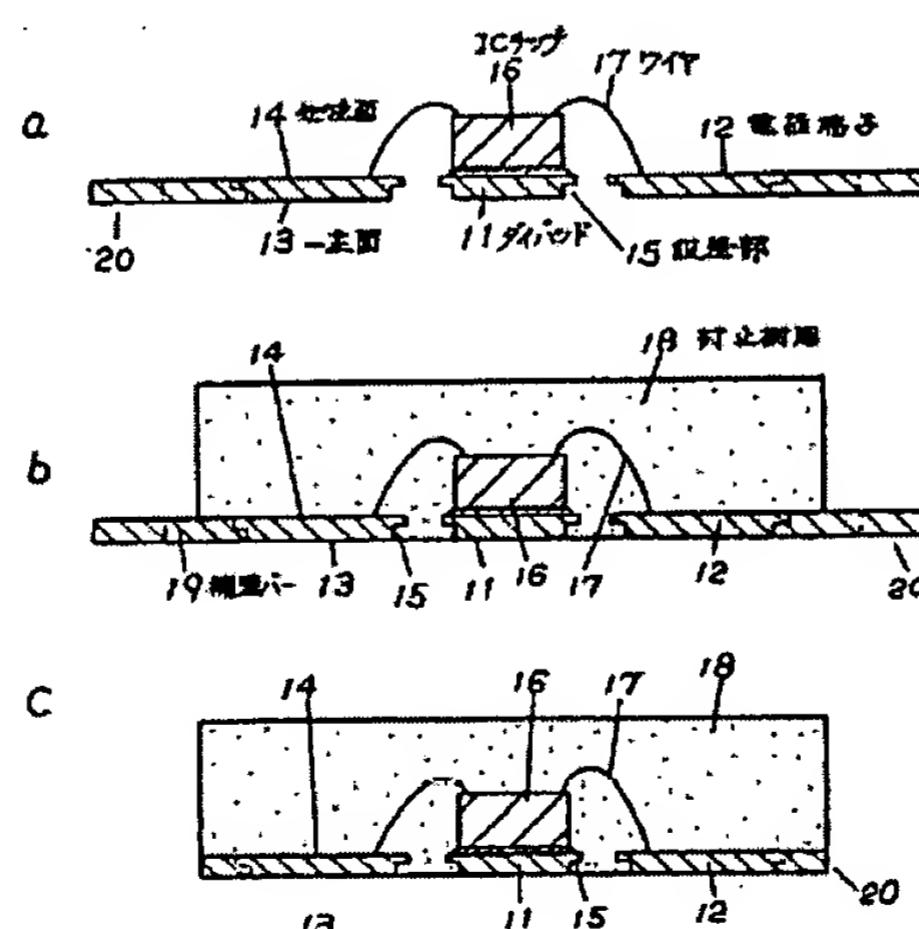


Figure 3

Key:

- 11 Die pad
- 12 Electrode terminal

- 13 One principal surface
- 14 Other principal surface
- 15 Step
- 16 IC chip
- 17 Wire
- 18 Sealing resin
- 19 Reinforcing bar

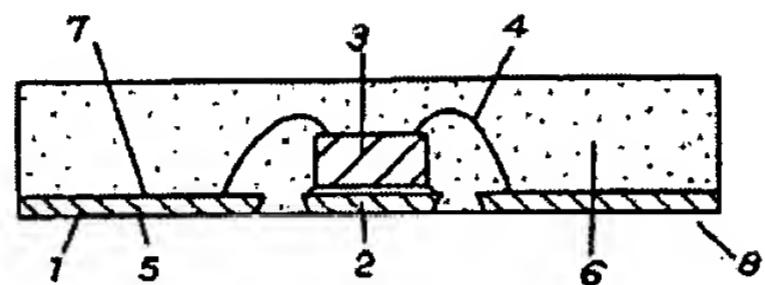


Figure 4



RALPH  
MCELROY TRANSLATION  
COMPANY

January 5, 2004

Re: 2098-96421

To Whom It May Concern:

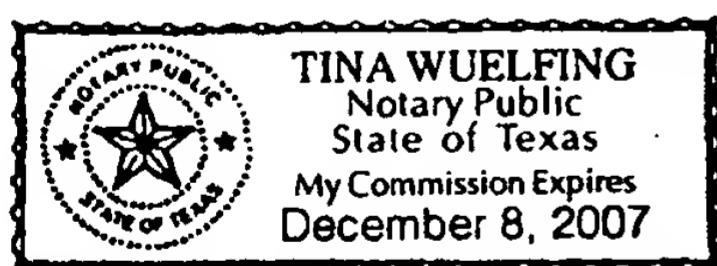
This is to certify that a professional translator on our staff who is skilled in the Japanese language translated the enclosed Kokai Patent Application No. Hei 1[1989]-106456 from Japanese into English.

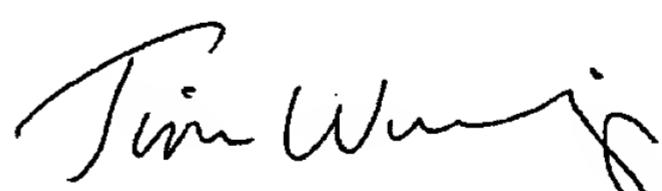
We certify that the attached English translation conforms essentially to the original Japanese language.

Kim Vitray

Kim Vitray  
Operations Manager

Subscribed and sworn to before me this 5th day of January, 2004.



  
\_\_\_\_\_  
Tina Wuelfing  
Notary Public

EXCELLENCE WITH A SENSE OF URGENCY®

910 WEST AVE.  
AUSTIN, TEXAS 78701  
[www.mcelroytranslation.com](http://www.mcelroytranslation.com)



(512) 472-6753  
1-800-531-9977  
FAX (512) 472-4591